

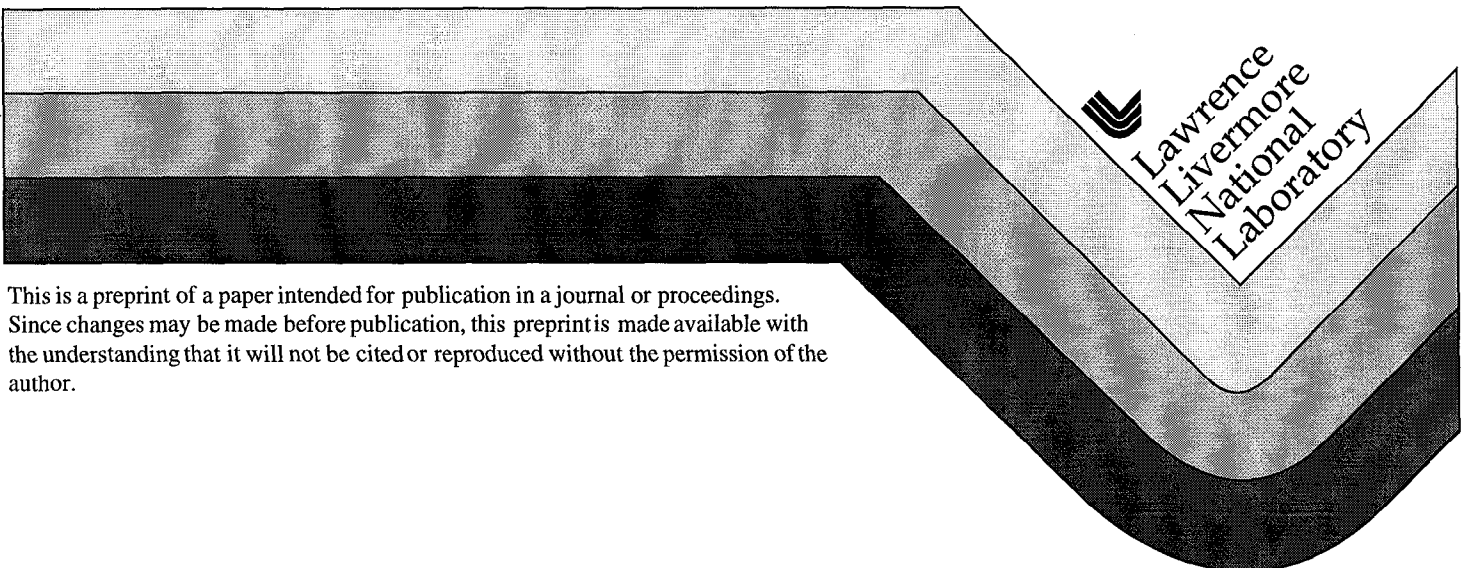
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PREPRINT

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Masks for extreme ultraviolet lithography

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ABSTRACT

In extreme ultraviolet lithography (EUVL), the technology specific requirements on the mask are a direct consequence of the utilization of radiation in the spectral region between 10 and 15 nm. At these wavelengths, all condensed materials are highly absorbing and efficient radiation transport mandates the use of all-reflective optical systems. Reflectivity is achieved with resonant, wavelength-matched multilayer (ML) coatings on all of the optical surfaces – including the mask. The EUV mask has a unique architecture - it consists of a substrate with a highly reflective ML coating (the mask blank) that is subsequently over-coated with a patterned absorber layer (the mask). Particulate contamination on the EUVL mask surface, errors in absorber definition and defects in the ML coating all have the potential to print in the lithographic process. While highly developed technologies exist for repair of the absorber layer, no viable strategy for the repair of ML coating defects has been identified. In this paper the state-of-the-art in ML deposition technology, optical inspection of EUVL mask blank defects and candidate absorber patterning approaches are reviewed.

INTRODUCTION

Extreme ultraviolet lithography (EUVL) is a leading candidate to succeed optical lithography for integrated circuit manufacturing. A demonstration lithography machine capable of producing 100 nm linewidth generation patterning is being designed and fabricated. This machine will have a 4 mirror, 4X reduction projection optical system with 0.1 NA. Two near-normal incidence mirrors are also used in the condenser. Each of these six near-normal incidence mirror surfaces is coated with Mo/Si multilayers designed to have highest reflectivity at 13.4 nm. Sweeney et al.¹ have described the details of the optics design, and Gwyn et al.² have described the more general technical program to develop EUVL for manufacturing.

Mask fabrication is one of the key challenges in EUVL. The mask blank is a silicon wafer substrate coated with 40 pairs of Mo and Si (a Bragg reflector) designed to maximize reflectivity at 13.4 nm. The mask blank is coated with an absorbing film that is patterned with the desired integrated circuit features using conventional mask patterning lithography followed by reactive ion etching. Technical approaches to fabricating EUVL mask blanks and to patterning mask absorber features are addressed in this paper.

MASK BLANK FABRICATION PROCESS

EUVL mask blanks are fabricated in a class 100 research clean-room at Lawrence Livermore National Laboratory. The facility contains a low defect density ion beam sputter deposition system for mask blank coatings and a variety of automated wafer inspection instruments. Routes of ingress and egress to all process tools and metrology instruments utilize class 1 mini-environments and standard mechanical interface (SMIF) wafer handling³.

EUVL mask blanks can be made from Si or glass substrates. Gianoulakis and Ray-Chaudhuri⁴ have studied some of the tradeoffs in the choice of mask blank substrates. Mask blanks are presently being fabricated with Si wafers as substrates. Mask blank processing begins with the manual unload of the wafer shipping containers in a HEPA filtered, laminar flow, class 1, auxiliary loading unit (ALU). The 150 mm Si wafers are left in their shipping cassettes and automatically loaded into a SMIF pod. SMIF handling is utilized throughout the remainder of the mask blank fabrication sequence. The wafers are examined with an unpatterned wafer inspection tool that uses normally incident laser illumination of the wafer surface as described by Altendorfer et al.⁵ During inspection the wafer handling systems of the inspection tool are used to transfer the

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wafers from shipping to SMIF processing cassettes. The system is equipped with two 150-mm SMIF stations. Station 1 is configured for wafer shipping cassettes, and station 2 is configured to accept SMIF standard processing cassettes. Scatter maps for each wafer are recorded and stored in a database. Next, the SMIF pod is moved to another bare wafer inspection tool that scans the sampling with grazing incidence illumination. Scatter maps are recorded for each wafer and stored in the database.

After inspection the SMIF pod is transferred to the ion beam deposition system (IBDS) for multilayer coating of the wafers. The deposition system has been described in detail in earlier publications by Vernon⁶ and Kearney⁷. A SMIF loader and cassette elevator are used to transfer the processing cassette into the system load-lock. The deposition system is configured for single wafer processing. Robotic handling is employed to transfer the wafers from the processing cassette to the deposition chamber. An ion beam sputter deposition process is used to sequentially sputter a high reflectance Mo/Si ML from elemental Mo and Si sputtering targets. After deposition the coated wafer is returned to the processing cassette and the process is repeated until all of the wafers have been coated. The load lock is vented with filtered, dry N₂, and the cassette elevator returns the processing cassette to the SMIF pod. After ML deposition optical scatter maps are recorded and stored in the database. As part of the inspection, the wafers are removed from the processing cassettes and reinserted into shipping cassettes. Subsequent processing is done on a wafer by wafer basis, so wafers are transferred manually from the shipping cassettes to individual carriers as required. At this point in the process, the database contains optical scatter maps of each wafer recorded before and after ML deposition. The data allows certification of mask blank defect density and a partitioning of substrate induced and process added defects.

The EUVL optical properties of the blank are derived from measurement of the wavelength dependent EUV reflectance. The measurements are made at the EUV reflectometer, beamline 6.3.2 at the Advanced Light Source (ALS) at Lawrence Berkeley National Laboratory⁸. The blanks are then ready for patterning.

MASK BLANK REFLECTIVITY

The EUVL mask is a multilayer reflector, and it should reflect as much of the incident radiation as possible. The reflectivity versus wavelength of a Mo/Si coating produced with ion beam sputter deposition with Si as the final layer is shown below in Figure 1. Using the ion beam sputter deposition technique, reflectivity of 65% is obtained compared to a theoretical maximum of 75%. The reason for the difference between theoretical and experimentally measured reflectivity is due to interface roughness, oxidation of the multilayer surface and intermixing of the layer materials⁹. The multilayer films can be deposited on silicon or glass substrates. The substrate influences the reflectivity through its surface roughness. If significant roughness at spatial frequencies higher than resolved by the EUV projection optics exist on the mask substrate, reflectivity will be reduced as described by Gullikson¹⁰.

In order to maintain maximum exposure intensity and adequate illumination uniformity in the wafer image field, the EUVL mask must reflect EUV light of the proper wavelength to match the wavelength bandpass of the projection optics system. The ETS optical system design described by Sweeney et al.¹ has six multilayer-coated mirrors (four imaging mirrors and two collection mirrors with multilayer coatings). The power that reaches the wafer is proportional to the integral of the product of the reflectivity versus wavelength for each mirror and the mask. This power, $P(d)$, is a function of the mask multilayer period, d .

$$P(d) = \int_{-\infty}^{\infty} \prod_{i=1, \dots, 6} R_i(\lambda) R_{\text{mask}}(\lambda, d) d\lambda \quad (1)$$

where $R_i(\lambda)$ is the reflectivity of mirror i and $R_{\text{mask}}(\lambda, d)$ is the reflectivity as function of wavelength and multilayer period for the mask. Figure 2 shows a calculation of the relative overlap integral of the ETS optical system reflectivity bandpass and the reflectivity of the mask for a range of mask multilayer period values. The model assumes ideal reflectivity versus wavelength response with no interface diffusion or roughness between the Mo and Si multilayer films. The model also assumes that the multilayer coating bandpass of each optical element besides the mask is perfectly matched to the design centroid wavelength of 13.4 nm. The variation of the overlap integral over a range of multilayer period values near the maximum overlap sets the uniformity of the mask pattern area coating response required for a given degree of intensity uniformity at the wafer plane. If the multilayer period is not uniform over the mask patterned area, the effective illumination intensity at the wafer will be affected according to the result plotted in Figure 2. With the ion beam sputter deposition system, 81 layer Mo/Si ML coatings that simultaneously exhibit a peak normal incidence reflectance of 65% or greater, with a centroid operating wavelength uniform to within $\pm 0.2\%$ over a 60 mm radius, can be routinely fabricated. Figure 3 shows a plot of centroid wavelength versus position over a 70 mm radius coated with Mo/Si multilayers.

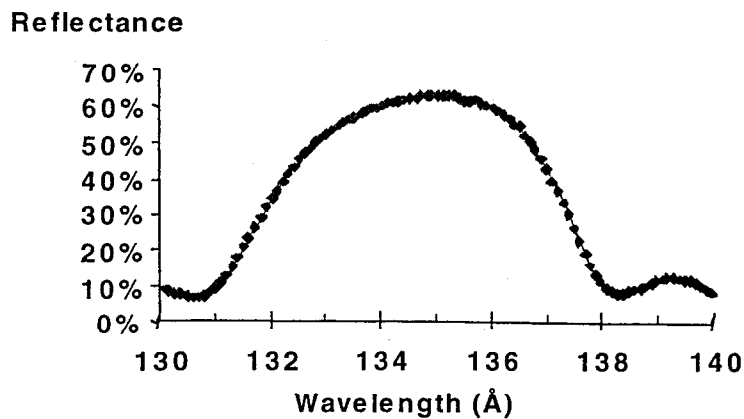


Figure 1. Reflectivity versus wavelength for a Mo/Si multilayer mask blank as measured by the beamline 6.3.2 reflectometer.⁷ The peak reflectivity is ~65%.

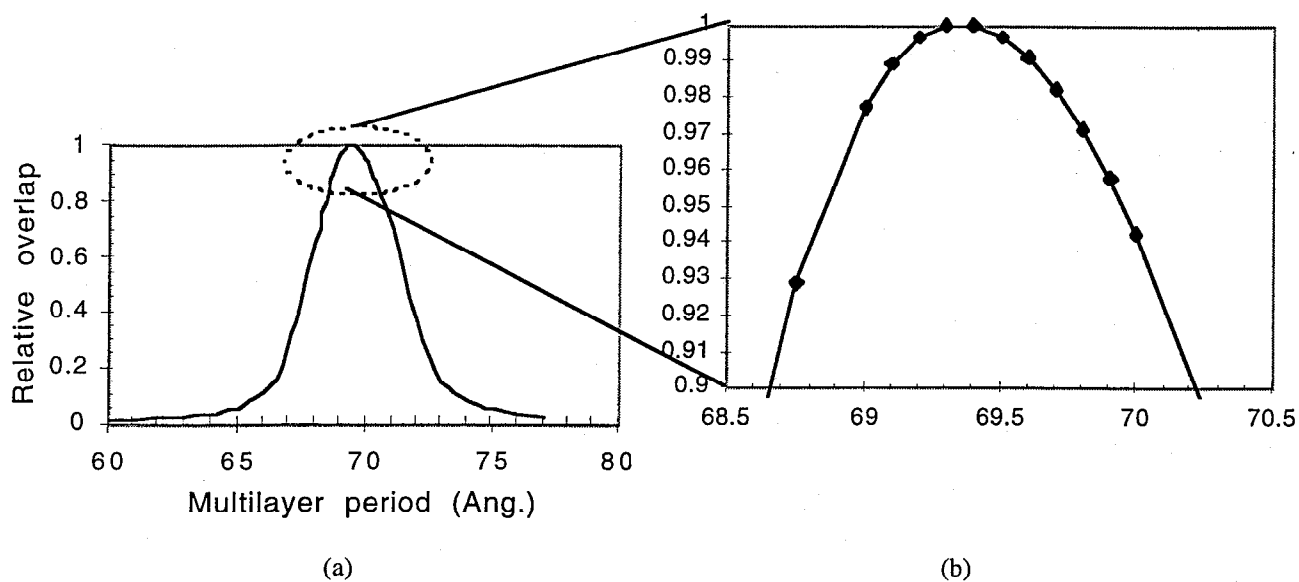


Figure 2. a) Plot of the overlap integral, $P(d)$, for an optical system with six multilayer coated mirrors (four imaging mirrors and two collection mirrors with multilayers) and a mask blank with multilayer period, d . b) Region around maximum of $P(d)$ expanded.

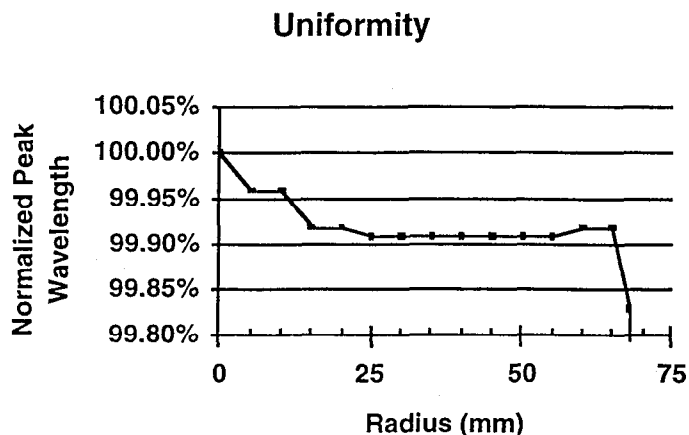


Figure 3. Plot of normalized centroid reflected wavelength uniformity measured over a 70 mm radius of a Mo/Si coating. The drop in wavelength around 65 mm occurs because the edge of the mask blank surface is shadowed by the clamp holding it during deposition.

DEFECT REDUCTION ON BLANKS

The EUVL mask is reflective. Flaws in the mask blank that alter the magnitude or phase of the reflected EUV fields enough to significantly alter the resist image in the lithographic process constitute printable defects. This is of considerable concern since, in contrast to absorber layers, there is, at present, no viable strategy for the repair of defects in the reflective regions. Hence, the mask blank must be free of printable defects. The actual printability of a particular mask blank "defect" depends in detail on several factors including: the magnification, flare, and coherence of the imaging system; the proximity of the defect to the printed feature; and the CD and shape of the feature involved. This said, preliminary theoretical models of mask defect printability by Lin et al.¹¹ indicate that, at a CD of 100nm, mask blank defects 30 nm in diameter, have the potential to print in the lithographic process. These simulations were performed using scalar theory and assuming that magnitude or phase is shifted abruptly by the defect. More rigorous modeling including simulation of EM propagation in the multilayer is being pursued. Initial more inclusive models that can be applied to defect simulation are described by Pistor et al.¹² and Bollepalli et al.¹³ Potential sources of mask blank defects include, in addition to process generated coating defects, substrate imperfections such as crystal oriented particles (COPs), dislocations, stacking faults, etc. that are replicated or partially replicated in the ML coating process. The identification, and classification of mask blank defects is a necessary prerequisite to engineering development of defect free mask blank fabrication protocols.

The roadmap for EUVL mask development is to reduce printable mask blank defect density by one order of magnitude per year. The roadmap requires that we produce mask blanks with a defect density of $10^{-1}/\text{cm}^2$ in 1998, reducing the defect density to $10^{-3}/\text{cm}^2$ in the year 2000. The minimum diameter of defects detected with inspection must also decrease from 130 nm in 1998 to 30 nm or better in 2000.

Significant progress has been made in improving the properties of the IBDS coatings to meet the EUVL mask blank development roadmap. Figure 4 shows the evolution of mask blank defect density with the number of wafers processed for a sequence of 300 wafers. The measurements were made with a detection threshold of 130 nm which is the limit of the equipment presently available at our facility. The defect count represents the number of defects added in the multilayer coating process and handling of blanks in the IBDS.

Defect density (cm^2)

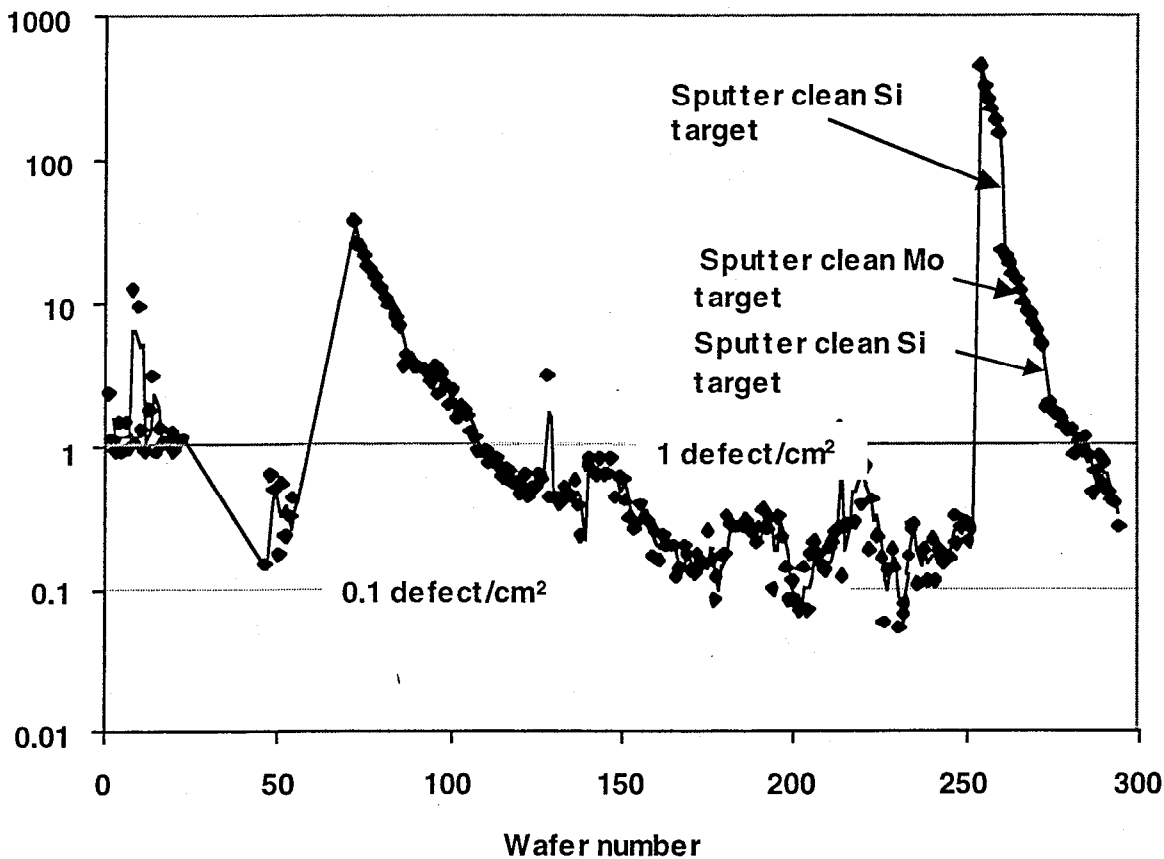


Figure 4. The density (defects/ cm^2) of defects with diameter ≥ 130 nm added in the IBDS coating process for a series of close to 300 EUVL mask blanks. The discontinuous increases in defect density coincide with major preventative maintenance (PM) operations. Following PM defect density decreases with the number of wafers processed.

Overall the defect density decreases with the number of wafers processed. The discontinuous increases in defect density observed at wafer number 50 and wafer number 250, are the result of major preventative maintenance (PM) operations. In each case, the defect density decreases with the number of wafers processed following the PM operation. The rate of decrease in defect density after PM was increased by using ion beam sputter pre-cleaning of the sputtering targets. The ion beam is defocused somewhat to cover the entire target surface, and the target is irradiated with ions for times on the order of the time required to grow a complete 40 layer pair stack. No mask blank is present during this operation. The drop in defect density versus sample number is greater after the last defect density peak shown in Figure 4. The ion beam targets were sputter-cleaned between samples at 3 points. The first two discontinuities in the curve correspond to sputter pre-cleaning of the Si target. The third, smaller discontinuity corresponds to sputter pre-cleaning of the Mo target. Note that the majority of wafers processed have total defect densities between 1 and 0.1 defects/ cm^2 .

The processed mask blanks contain defects that arise from several contributions: defects that are on the substrate that are replicated in the ML coating process, particles that are added by the wafer handling systems used to move the wafers into and out of the IBDS processing chamber and defects added in the thin film deposition process. Pre-measurement of the Si substrates, periodic scanning of monitor wafers used to assess handling induced contamination, and inspection of the fully processed blanks permits us to segregate the contributions of these sources to the total defect density. For blanks with order 0.1 defects/ cm^2 , the relative contributions of substrate defects, defects from automated handling in the IBDS and handling in

post-coating defect inspection, and defects added in the sputtering process to the average mask blank defect density are 0.06, 0.06, and 0.04 defects/cm², respectively. Note that, on average, substrate and handling induced contamination combine to yield defect densities of 10⁻¹/cm².

INSPECTION FOR MASK BLANK DEFECTS

EUVL mask defect reduction efforts are targeted at eliminating "printable" mask blank defects. Four times reduction EUVL printing tools that provide the ultimate experimental test of defect printability for EUVL will be available for printing studies in several years; in the interim, we are relying on optical inspection to guide the mask blank defect reduction program. Even with production quality 4X lithography systems, mask blank manufacturing will continue to employ visible light scattering as a means to detect defects on EUVL mask blanks. The mask blank fabrication facility is equipped with two models of bare wafer inspection tools. The principles of operation of the latter model is described by Altendorfer et al⁴. For bare Si, the minimum detection threshold of these instruments is 130 and 80 nm respectfully. The instruments are calibrated by depositing polystyrene latex (PSL) spheres of a known size on Si wafers and Mo/Si ML coated mask blanks, and measuring the optical scatter. The detection threshold of both systems is 130 nm for Mo/Si ML coated blanks.

Efforts are also underway to detect defects in mask blanks using EUV light. Jeong et al¹⁴. describe recent progress in the development of an EUV scatterometer for mask blank metrology in these proceedings. The main focus of present efforts in EUV detection of defects is to correlate scattering at EUV wavelengths with scattering at optical wavelengths so that optical scattering can be relied upon as the principal means for mask blank defect detection.

MASK ABSORBER PATTERNING

The EUVL mask blank consists of a multilayer stack deposited on a silicon wafer substrate as described above. Tennant et al¹⁵. described several approaches to mask patterning—including etching the multilayer stack, reducing multilayer reflectivity with ion beam damage, and depositing a patterned absorber film on top of the multilayer stack. The latter approach is the most manufacturable.

Although no method is presently available to repair defects in or beneath the multilayer stack, the patterned mask absorber can be repaired with standard focused ion beam methods. However, focused ion beam repair may damage the multilayers in the repaired region as first described by Hawryluk and Stewart¹⁶. Hawryluk et al¹⁷. later demonstrated that a buffer layer of silicon deposited between the top of the resonant multilayer stack and the absorber material and the use of 10 kV neon ions from a gas field ion source could be used to repair the absorber without damage to the multilayer. Silicon dioxide has also been used as a buffer layer material. Yan et al¹⁸. have recently studied the feasibility of repairing aluminum absorbers on oxide buffer layers. Because the buffer material absorbs EUV radiation, it may be necessary to remove it after repair.

The processing steps in fabricating a patterned absorber on the EUVL mask are listed below.

- 1) Repair buffer layer deposition
- 2) Absorber layer deposition
- 3) Resist coating
- 4) Resist exposure
- 5) Resist development
- 6) Resist linewidth measurement
- 6) Pattern transfer (from resist into absorber)
- 7) Resist removal
- 8) Absorber linewidth measurement
- 9) Absorber pattern image placement measurement
- 10) Defect inspection
- 11) Defect Repair
- 12) Buffer layer etch

Cleaning of the absorber might be performed at various points in the process flow, and several iterations of repair and defect inspection could be performed. Because EUVL masks are made on standard Si wafer substrates, equipment for performing all of these process steps is readily available. Moreover, the equipment available is designed to meet the stringent requirements of leading edge semiconductor device fabrication on wafers; therefore, EUVL mask patterning can be performed with equipment that may be better suited to patterning smaller linewidths and for finding and controlling smaller defects than present optical lithography mask fabrication equipment.

The EUVL mask absorber should attenuate all or nearly all of the incident beam. Most materials with thickness less than 500 nm absorb most of the incident EUV radiation with wavelengths from 10 to 15 nm. Figure 5 shows a plot of calculated transmissivity of several elements and silicon dioxide at 13.4 nm wavelength. The transmissivity was calculated using optical constants tabulated by Henke et al.¹⁹ and using textbook bulk density values for the compounds. Aluminum has been used as an absorber for recent EUVL mask experiments. Experiments are also in progress to investigate alternative absorber materials.

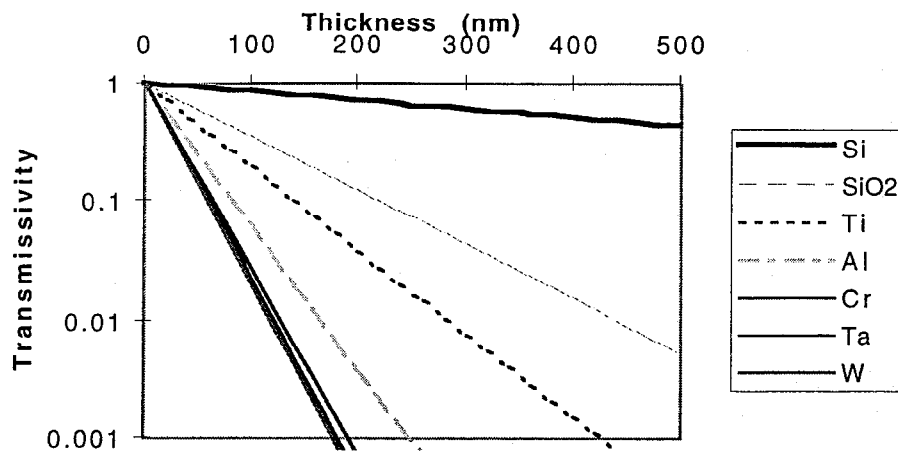


Figure 5. Log plot of calculated transmissivity of several elements at 13.4 nm wavelength. The elements are listed in the legend in order of decreasing transmissivity.

The absorber film must not only attenuate the EUV radiation, but it must also be readily etched, inspected, repaired, and cleaned. The requirements for absorber materials are also driven by these process steps. Absorbers must be vacuum compatible so that they do not outgas during mask usage. Materials that are easily patterned with reactive ion etching (RIE) and that can be cleaned with aggressive wet and or dry cleaning are typically robust in vacuum. A unique aspect of EUVL mask absorber material processing is that the mask must be processed at temperatures less than 150°C. Mirkarimi and Montcalm²⁰ have shown that reflectivity of Mo/Si multilayers decreases significantly with temperature above 150°C. This reflectivity decrease for Mo/Si multilayers is probably due to stress relief that results in multilayer period change and due to the formation of molybdenum silicides at the interfaces between the multilayer materials. Rosen et al.²¹ have studied these effects in detail. The process for fabricating the EUVL mask absorber must therefore be performed at temperatures where reflectivity is not significantly reduced. Figure 6 shows a cross section of an aluminum absorber pattern on a Mo/Si multilayer with an oxide buffer layer. The buffer layer has been removed from clear areas. Reflectivity of the Mo/Si multilayer was measured before and after processing. The peak reflectivity of the multilayer was not reduced, and the centroid wavelength was changed by less than 0.025 nm. Although optical projection lithography was used to pattern the aluminum absorber features shown in Figure 6, experiments by Hawryluk et al.²² indicated that e-beam lithography may also be used.

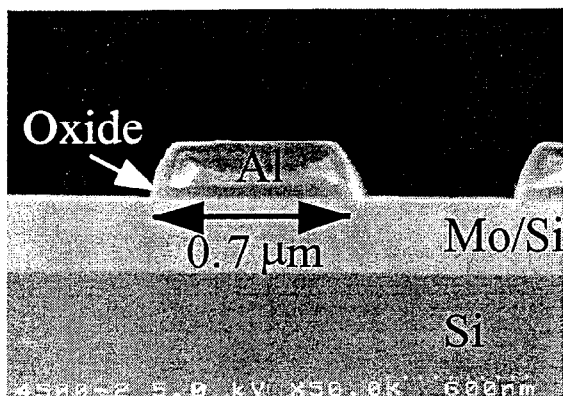


Figure 6. Scanning electron micrograph of a cross section of an EUVL mask with aluminum absorber on a Mo/Si multilayer.

A small field exposure system with 10X reduction and 0.08 NA described by Goldsmith et al.²³ has been used to image prototype EUVL masks with Mo/Si multilayers and Al absorbers. Figure 7 shows lines and spaces patterned in a 80 nm thick film of DUV resist. Resolution of 100 nm equal lines and spaces and 70 nm lines on a 210 nm pitch is clearly evident. These results indicate that the aluminum absorber process in combination with small field EUV imaging can provide early learning for absorber patterning process development, programmed defect experiments, and absorber repair feasibility studies.

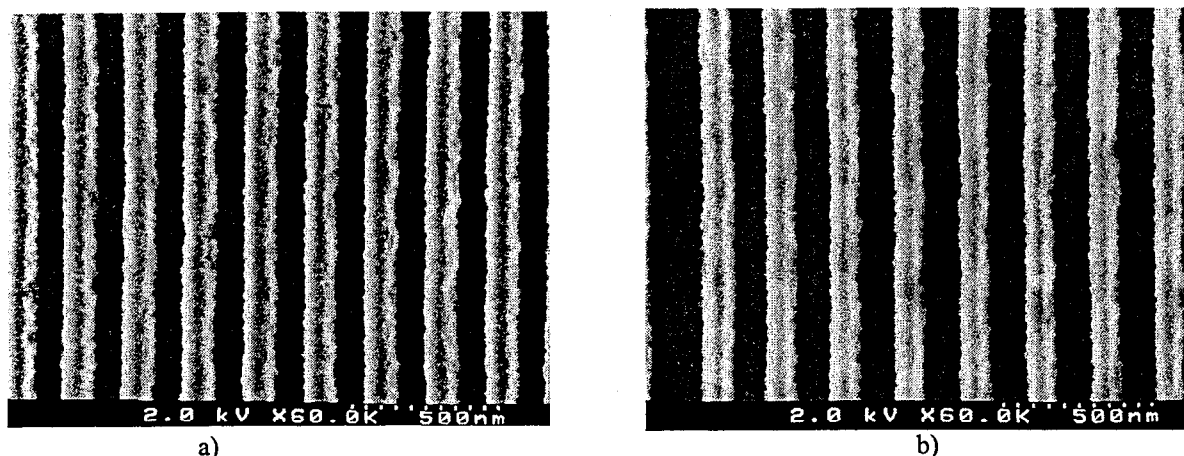


Figure 7. a) 100 nm equal lines and spaces and b) 70 nm lines with 210 nm pitch exposed in 80 nm of DUV resist using a 10X reduction 0.08 NA small field imaging system.

The mask must be maintained defect free during use on the exposure machine and in storage and handling. Most material candidates for pellicles significantly attenuate EUV wavelengths. Silicon is relatively transparent at 13.4 nm wavelength; however, silicon attenuates 57% over a 500 nm thickness. Hence, a pellicle similar to that used in optical lithography may not be acceptable because of reduced throughput. Other methods of protecting the mask during exposure, handling and storage are under investigation by others and will be described in a future publication.

Experiments to determine the minimum printable absorber defect by Yan et al.²⁴ have indicated that ~60 nm clear defects (e. g. a break in a line) and ~80 nm opaque defects (e. g. extra absorber attached to the line) may change the linewidth of 100 nm features by more than ± 3.3 nm. Inspection of the patterned absorber is feasible using e-beam or photon-beam techniques. Experiments have indicated that inspection with e-beam using secondary electron signal contrast is feasible although a long time is required to inspect a 104 by 130 mm area. Use of photon-based methods to inspect the patterned absorber are also under investigation.

CONCLUSION

Technical approaches to EUVL mask blank fabrication and pattern definition have been described. Further progress in reducing mask blank defect density, patterning with linewidth and placement control, and inspecting and repairing defects on EUVL masks is necessary.

ACKNOWLEDGMENTS

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